REMARKS

1. The Examiner has required applicant under 37CFR 1.105 to "provide details of the sale of the "apparatus with features similar to the apparatus shown in Figure 1" (Specification page 12, lines 1-5) including proof of the date said apparatus was published for sale. Applicant is further expected to provide a specification, including Figures, for said apparatus which may be satisfied by the marketing materials for said apparatus."

Applicant does not understand what the Examiner is requesting in the quotation above. If the Examiner is requesting a patent specification of the unit that applicant sold more than one year prior to the filing date of this application, the Examiner may assume that applicant's prior unit was identical to the unit of this application except that the wafer 16 in the prior unit engaged the electrode 22. The circuit equivalent of this previous arrangement is shown in Figures 5a and 5b and is indicated in the specification as being prior art. Applicant has indicated in the specification that the separation of the wafer 16 and the electrode 22 constitutes a distinct advance over the prior art. This may be seen from the showing in Figures 4a and 4b and from the discussion on page 13, line 14 to page 15, line 13 of the specification. The discussion on pages 13-15 of the specification is especially significant since the prior art cited by the Examiner against the claims in the application do not relate at all to applicant's invention as set forth by applicant on pages 13-15.

Applicant's assignee of record has incorporated this invention in embodiments which applicant's assignee sold after the date of this application. These embodiments have been designated by applicant's assignee by the trademark "SHAMROCK." For the record, the Examiner should be aware that applicant's assignee has sold SHAMROCK equipment for years. Applicant's assignee has continuously made improvements in the SHAMROCK equipment throughout the years. Applicant's assignee has not provided, and does not provide, a new designation or a new model number for the SHAMROCK equipment every time that applicant's assignee makes a change in the SHAMROCK equipment. This means that the equipment designated by applicant by the mark SHAMROCK has been sold through a considerable number of years with progressive changes in the equipment.

2. Applicant has made changes in the specification to eliminate any confusion with respect to the designations 30 and 34. The changes in the specification have not required any changes in the drawings.

3. In paragraph 10 of the Office Action, the Examiner appears to indicate that applicant has not disclosed the first electrical conductor and the second electrical conductor recited in the claims. Applicant respectfully disagrees with the Examiner. The first electrical conductor is the plate 30 and the second electrical conductor is the ring 32. Applicant has amended the specification to indicate that the plate 30 may be considered as an electrical conductor and the ring 32 may be considered as an electrical conductor.

4. Applicant has made changes in the claims to correct informalities noted by applicant's attorney upon a further study of the claims. Applicant respectfully submits that these changes are supported by the specification and the drawings as originally filed and that these changes are consistent with the specification and the drawings in the application as originally filed. Applicant also respectfully submits that the claims as now written are definite.

5. The Examiner has rejected claims 1-21 on the following basis:

> "Applicant has not provided sufficient teaching of how a wafer can be "spaced" from both electrodes and any physically supporting surfaces."

Applicant has not disclosed or claimed that the wafer is spaced from any physically supporting surfaces. Applicant has disclosed only that the wafer is spaced from the first and second electrodes. Applicant respectfully submits that, based upon applicant's disclosure in the specification and in the drawings, a person of ordinary skill in the art would know how to space, and even closely space, the wafer 16 from the electrode 22. This would particularly apply to claims 7, 14 and 21.

"Spaced" ↕ placed on top of ✓

6. The Examiner has rejected claim 9 on the basis that it is based on a disclosure which is not enabling. Applicant does not understand from paragraph 3 of the Office Action why claim 9 is based upon a disclosure that is not enabling. However, applicant has amended claim 9 to recite that the first electrical conductor is disposed in a spaced relationship to the first electrode and that the second electrical conductor is disposed in a spaced relationship to the

P.4 Amend. OK ✓

second electrode. The same comments apply to claims 16 and 20. Applicant had also amended the specification to indicate that the ring 30 and the plate 32 may be respectively considered as the first and second electrical conductors.

7. Claims 1-4, 7, 8, 11, 14, 15, 19 and 21 have been rejected under 35 U.S.C. 102(b) as being anticipated by Koshimizu patent 5,980,687. As now written, claims 1-4, 7, 8, 11, 14, 15, 19 and 21 are allowable for certain important reasons over Koshimizu. By way of illustration, applicant provides all of the elements recited in claim 1 to process a single wafer. Koshimizu simultaneously processes two (2) wafers. Koshimizu provides the elements 116, 118, 122 and 134 to process an upper wafer in Figure 1 and provides the elements 108, 110, 114 and 130 to process a lower wafer in Figure 1. As will be seen, Koshimizu discloses only one electrode to process each wafer.

Apparatus is recited in claim 1 that a wafer is being etched. To etch a wafer, Koshimizu provides only the electrode 116, and does not provide a second electrode, to process the upper wafer. The same reasoning applies to the lower wafer. Furthermore, Koshimizu does not disclose that a first electrode and magnetic members are disposed relative to each other and to molecules of an inert gas for ionizing the molecules of the inert gas. Since Koshimizu does not disclose a second electrode for either the upper wafer or the lower wafer, there is also no disclosure in Koshimizu that the second electrode and the wafer are disposed relative to each other, and the second electrode is constructed, to obtain a movement of the ions to the surface of an insulating layer on the wafer at the low and controlled speed. Claims 2-4, 7, 8, 11, 14, 15, 19

and 21 are allowable over Koshimizu for similar reasons since Koshimizu does not disclose first and second electrodes for providing an etching of a low magnitude on an insulating surface of a wafer.

8. Claims 5, 6, 10, 12, 13, 17, 18 and 20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Koshimizu as applied to claims 1-4, 7, 9, 11, 14, 15, 19, and 21 and further in view of Novak patent 6, 220,201. Claims 5, 6, 10, 12, 13, 17, 18 and 20 are dependent from respective ones of claims 1,7 and 14. Because of this, claims 5, 6, 10, 12, 13, 17, 18 and 20 are allowable over Koshimizu for the same reasons as discussed above in paragraph 7. Claims 5, 6,10, 12, 13, 17, 18 and 20 are also allowable over Novak for the same reasons. Since neither Koshimizu nor Novak discloses the same features recited in the claims, Koshimizu and Novak cannot be combined to reject claims 5, 6, 10, 12, 13, 17, 18 and 20.

Certain of claims 5, 6, 10, 12, 13, 17, 18 and 20 are allowable over the combination of Koshimizu and Novak for other reasons of same importance. For example, claim 5 recites that first and second electrically conductive members are respectively adjacent to, but spaced from, the first and second electrodes at a reference potential to provide for the creation of electrical fields respectively between the first electrode and the first electrically conductive member and between the second electrode and the second electrically conductive member. Neither Koshimizu nor Novak discloses first or second electrically conducting members such as recited in claim 5. Similar recitations appear in such claims as claims 6, 13, 16 and 20. Because of this, neither Koshimizu nor Novak can disclose that an electrical field is created between the

first electrode and the first electrically conductive member or between the second electrode and the second electrically conductive member.

9. Applicant has retained claim 1-42 in the application, a number of them in at least slightly amended form. Applicant has added claims 43-51 by this amendment. Claims 43-51 are dependent from claim 21. Claim 21 is allowable over the combination of Koshimizu and Novak because neither reference discloses or suggests first and second electrodes for operating on a wafer to obtain a smooth and even etching of a surface of an insulating layer in the wafer at a low rate without any pits on the surface of the insulating layer. Claim 21 is additionally allowable once the combination of Koshimizu and Novak in reciting a supply of molecules of an inert gas for introduction into the enclosure to cooperate with the first and second electrodes and the magnetic members in obtaining an ionization of the gas molecules in the enclosure by the electrical and magnetic fields in the enclosure and in obtaining a movement of the ions in the enclosure to the wafer at a low speed to obtain a smooth and uniform etching of the surface of the insulating layer at a low rate without any pits in the surface of the insulating layer.

Claims 43-51 are allowable over Koshimizu and Novak, individually or in combination, because they are dependent from allowable Claim 21. Claims 43-51 are also allowable over the references, individually or in combination, for other reasons of some importance. For example, neither Koshimizu nor Novak discloses or suggests that the first electrode provides the high electrical field in cooperation with the magnetic field for producing an ionization of molecules of an inert gas in the enclosure or that the second electrode provides

the low electrical field in cooperation with the magnetic field for etching the surface of the insulating layer on the wafer to obtain the smooth and uniform etching on the surface of the insulating layer at the low rate without any pits in the surface of the insulating layer. This combination is recited in claim 43.

Claim 45 recites that a first electrical conducting member is disposed in a co-operative relationship with the first electrode to provide for the production of the high electrical field and that a second electrical conducting member is disposed in cooperative relationship with the second electrode to provide for the production of the low electrical field. Neither Koshimizu nor Novak discloses these features. Claim 47 is allowable over Koshimizu and Novak because it is indirectly dependent from Claim 45 and because it further defines the relationship between the electrodes and the electrical conducting members.

Neither Koshimizu nor Novak discloses or suggests the features recited in Claim 48. For example, neither reference discloses or suggests that the wafer and the first electrode define a series relationship between two (2) capacitors, one having a high capacity impedance and the other having a low capacity impedance and that the high capacity impedance limits the energy providing for the etching of the surface of the insulating layer in the wafer.

10. The Examiner has made the following statement at the bottom of page 7 of the Office Action:

> "In particular, it has been established that apparatus claims as opposed to method claims must distinguish from the prior art in terms of structure rather than function. See MPEP 2114. In particular, the "Manner of operating the device does not differentiate apparatus claims from the prior art.""

The Examiner has made this statement without reference to any specific claim. Claim 21 is probably a good claim to show how the Examiner is not correct in his interpretation of applicant's claims. The recitation of the last paragraph in claim 21 does not recite a "manners of operating the device." Rather, it recites a cooperative relationship between different elements in applicant's apparatus for producing results not previously achieved in the prior art. There is nothing in MPEP 2114 that indicates that the recitation in the last paragraph of claim 21 specifies a "manner of operating the device."

Furthermore, applicant respectfully submits that the Examiner has misinterpreted MPEP 2114. MPEP 2114 does not prevent applicant from distinguishing over the prior art by functional language. MPEP2114 specifies only that a claim having functional language can be rejected if the prior art apparatus teaches all of the structure of the claim. The prior art references cited by the Examiner do not teach all of the structure recited in claim 21 or the other claims. For example, the prior art references do not disclose or suggest first and second electrodes for etching a wafer. Furthermore, the prior art references do not disclose or suggest a supply of molecules of an inert gas for introduction into the enclosure and cooperative with the first and

second electrodes in the structure for providing the functions recited in the claim. The underlining has been provided to emphasize that different elements are being recited and that these elements are cooperative to obtain the specified results. Furthermore, the prior art references do not obtain the same results as applicant or any results at all close to the results obtained by applicant.

11. In order for different prior art reference to be combined to reject a claim, the references have to disclose or suggest the combination recited in the claim. *ACS Hospitality Systems, Inc. v. Montefiore Hospital,* 732 F.2d 1572, 221 USPQ 929 (Fed. Cir. 1984). As the Federal Circuit indicated in the *ACS* case at 732 F.2d 1577, 221 USPQ 933:

> "Obviousness cannot be established by combining the techniques of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under Section 103, teaching of references can be combined only if there is some suggestion or incentive to do so."

Neither of the references cited by the Examiner to reject claims 5, 6, 10, 12, 13, 17, 18 and 20 discloses or suggests certain of the features recited in the claim. The references accordingly cannot be combined to reject the claims.

12. Applicant notes that the Examiner has not acted on claims 22-42. Applicant respectfully requests the Examiner to act on claims 22-42 in the next Office Action. Since this

will be the first Office Action with respect to claims 22-42, applicant respectfully submits that the next Office Action should not be a final rejection if the Examiner rejects any of these claims.

13. Reconsideration and allowance of the application are respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned **"Version with Markings to Show Changes Made"**.

Please charge any additional fees in connection with this amendment to our deposit account No. 06-2425.

Respectfully submitted,

Ellsworth R. Roston

Ellsworth R. Roston, Registration No. 16,310
Attorney for Applicants

FULWIDER PATTON LEE & UTECHT, LLP
6060 Center Drive, Tenth Floor
Los Angeles, California 90045
Telephone: (310) 824-5555
Facsimile: (310) 824-9696

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Page 5, lines 14-15:

Figure 2 is an enlarged fragmentary simplified schematic elevational view of the construction of a wafer[, and];

Page 7, lines 11-17:

The insulating layer 14 may illustratively have a thickness of approximately three (3) microns. The sockets 18 may be completely, or partially, formed through the thickness of approximately three (3) microns in the insulating layer 14. Figure 2 illustratively shows the sockets 18 as extending completely through the thickness of the insulating layer 14. The preferred apparatus 10 of this invention illustratively may etch approximately one hundred angstroms (100 Å) from the surface 12 of the insulating layer[s] 14 in a smooth and even layer and without any pits in the layer.

Page 8, lines 1-11:

The apparatus 10 includes an enclosure 20 which may be formed in part by an electrode 22, an electrode 24 displaced from, but preferably substantially parallel to, the electrode 22 and magnets 26 and 28 disposed in a transverse (preferably substantially perpendicular) relationship to the electrodes 22 and 24. The electrode 22 is disposed in a contiguous but spaced and

substantially parallel relationship to the wafer 16 and is movable in position toward or away from the wafer, as indicated by a double-headed arrow 25. The spacing between the wafer 16 and the electrode 22 may illustratively be in the order of 0.1 - 2mm. A plate 30 extending from the magnet 26 in a substantially parallel and adjacent, but spaced, relationship to the electrode 22 also defines the enclosure 20. A ring 32 extending from the magnet 28 to a position spaced from, but [contiguous] adjacent to, the electrode 24 also defines in part the enclosure 20. The plate 30 and the ring 32 may be considered as electrical conductors.

Page 9, line 17 - page 10, line 5:

A conduit 44 is provided for introducing molecules of an inert gas such as argon into the enclosure 20 from a source 45. The argon molecules pass into the enclosure [3]20 through the space between the electrode 24 and the ring 32. The argon molecules pass out of the enclosure [3]20 through the space between the plate 3[4]0 and the wafer 16. The argon gas flow through the enclosure [3]20 may illustratively be at a flow rate of 0.1-50 SCCM at a working pressure of 0.5-5mTorr. The movement of the argon molecules through the enclosure 20 is facilitated by a vacuum pump 47.

IN THE CLAIMS:

1. (Amended): In combination for etching an insulating layer in a wafer to present a clean and fresh surface on the insulating layer for deposition,

a conduit for molecules of an inert gas,

a first electrode biased to a first voltage and spaced from the wafer,

a second electrode biased to a second voltage lower than the first voltage and spaced from the first electrode and the wafer,

magnetic members providing a magnetic field,

the first electrode and the magnetic members being disposed relative to each other and to the molecules of the inert gas for ionizing the molecules of the inert gas, and

the second electrode and the wafer being disposed relative to each other and to the ions of the inert gas, and the second electrode being constructed, to obtain a movement of the ions to the wafer at a low and controlled speed for an etching of the surface of the insulating layer by the ions at [the] a low and controlled speed.

5. (Amended): In a combination as set forth in claim 1,

the wafer being at a floating potential,

there being first and second electrically conductive members [respectfully] respectively adjacent, but spaced from, the first and second electrodes at a reference potential to provide for

the creation of electrical fields respectively between the first electrode and the first electrically conductive member and between the second electrode and the second electrically conductive member.

6. (Amended): In a combination as recited in claim 2,

a first source of alternating voltage for creating the bias on the first electrode, the bias on the first electrode being a negative direct voltage,

a second source of alternating voltage for creating the bias on the second electrode, the bias on the second electrode being a negative direct voltage,

the first electrode being disposed in a substantially parallel and contiguous relationship to the wafer,

there being a path for the flow of the [argon] molecules <u>of the inert gas</u> from the vicinity of the first and second electrodes and the magnetic members,

the wafer being at a floating potential,

there being first and second electrically conductive members respectfully adjacent, <u>but spaced from,</u> the first and second electrodes at a reference potential to provide for the creation of electrical fields respectively between the first electrode and the first electrically conductive member and between the second electrode and the second electrically conductive member.

7. (Amended): In combination for etching an insulating layer in a wafer to present a clean and fresh surface on the insulating layer for deposition,

an enclosure defined by magnetic members forming a magnetic field and by first and second electrodes spaced from each other and from the wafers and providing electrical fields,

a supply of molecules of an inert gas for introducing the molecules into the enclosure,

a first source of an alternating voltage for producing a direct negative voltage of a high magnitude on the first electrode for the creation of a first electrical field of a high magnitude in the enclosure,

a second source of an alternating voltage for producing a direct negative voltage of a low magnitude on the second electrode for the creation of a second electrical field of a low magnitude in the enclosure,

the molecules of the inert gas in the enclosure being ionized by the combination of the electrical and magnetic fields, and

the wafer being disposed relative to the second electrode and relative to the [argon] ions <u>of the inert gas</u> in the enclosure to receive an etching of a low magnitude on the surface of the insulating layer by the [argon] ions <u>of the inert gas</u> in the enclosure.

9. (Amended): In a combination as set forth in claim 7,

a first electrical conductor disposed in adjacent but spaced relationship to the first electrode at a particular reference potential to produce a first electrical field between the first electrode and the first electrical conductor, and

a second electrical conductor disposed in adjacent but spaced relationship to the second electrode at the particular reference potential to produce a second electrical field between the second electrode and the second electrical conductor.

11. (Amended): In a combination as set forth in claim 7,

the wafer being disposed in a spaced, but [contiguous] adjacent, relationship to the second electrode to create a first capacitor between the second electrode and the wafer and to create a second capacitor between the wafer and the ions of the inert gas in the enclosure.

13. (Amended): In a combination as set forth in claim 10,

a first electrical conductor disposed in adjacent, but spaced, relationship to the first electrode at a particular reference potential to produce a first electrical field between the first electrode and the first electrical conductor,

a second electrical conductor disposed in adjacent relationship, but spaced, to the second electrode at the particular reference potential to produce a second electrical field between the second electrode and the second conductor[.],

the wafer being disposed in a spaced, but [contiguous] adjacent, relationship to the second electrode to create a first capacitor between the second electrode and the wafer and to create a second capacitor between the wafer and the ions of the inert gas in the enclosure.

14. (Amended): In combination for etching an insulating layer in a wafer disposed in an enclosure to present a clean and fresh surface on the insulating layer for deposition,

magnetic members defining a magnetic field in the enclosure,

a first source of an alternating voltage for providing a first electrical field of a high magnitude in the enclosure,

a first electrode forming a part of the enclosure and connected to the first source of voltage for providing a negative DC voltage of a relatively high magnitude at a first position in the enclosure,

a second source of an alternating voltage for providing a second electrical field of a low magnitude in the enclosure,

a second electrode forming a part of the enclosure and connected to the second source of the alternating voltage for providing a negative DC voltage of a relatively low magnitude at a second position displaced from the first position and the wafer but near the [first] wafer,

a conduit for introducing molecules of an inert gas into the enclosure for ionization by the combination of the electrical and magnetic fields to produce ions of high density,

the second electrode and the wafer providing a first capacitor of a high impedance, and the wafer and the ions in the enclosure providing a second capacitor of a low impedance, in a circuit to produce a current of a low magnitude for etching the surface of the insulating layer in the wafer.

16. (Amended): In a combination as set forth in claim 14,

a first electrically conductive member disposed in an adjacent but spaced relationship to the first electrode and having a reference potential to provide an electrical field between the first electrode and the first electrically conductive member, and

a second electrically conductive member disposed in an adjacent but spaced relationship to the second electrode and having the reference potential to provide an electrical field between the second electrode and the second electrically conductive member.

18. (Amended): In a combination as set forth in claim 17,

the conduit being disposed adjacent, but spaced from, the first electrode to introduce the molecules of the inert gas into the enclosure and the molecules and ions of the inert gas being passed from the enclosure at a position adjacent to, but spaced from, the second electrode.

19. (Amended): In a combination as set forth in claim 14, the magnetic members being disposed in a direction substantially perpendicular to the first and second electrodes to produce a

helical movement of electrons in the enclosure and to provide for the production of the ions from the molecules of the inert gas by the electrons in the helical movement [of the electrons].

20. (Amended): In a combination as set forth in claim 1[3]4, a first electrically conductive member disposed in adjacent but spaced relationship to the first electrode and having a reference potential to provide an electrical field between the first electrode and the first electrically conductive member,

a second electrically conductive member disposed in adjacent but spaced relationship to the second electrode and having the reference potential to provide an electrical field between the second electrode and the second electrically conductive member,

the wafer having a floating potential and being disposed between the first and second electrodes in closer proximity to the second electrode than to the first electrode and being substantially parallel to the first and second electrodes,

the conduit being disposed adjacent, but spaced from, the first electrode to introduce the molecules of the inert gas into the enclosure and the molecules and ions of the inert gas being passed from the enclosure at a position adjacent to, but spaced from, the second electrode,

the magnetic members being disposed in a direction substantially perpendicular to the first and second electrodes to produce a helical movement of electrons in the enclosure and to

provide for the production of the ions from the molecules of the inert gas by the electrons in the helical movement [of the electrons].

21. (Amended): In combination for etching an insulating layer in a wafer to present clean and fresh surfaces on the insulating layer for deposition,

an enclosure defined by first and second electrodes displaced from each other and from the wafer for producing electrical fields in the enclosure and further defined by magnetic members for producing a magnetic field in the enclosure,

a first voltage source for producing a voltage of a high magnitude in the vicinity of [on] the first electrode to obtain a production of a high electrical field in the enclosure,

a second voltage source for producing a voltage of a low magnitude in the vicinity of [on] the second electrode to obtain a production of a low electrical field in the enclosure, and

a supply of molecules of an inert gas for introduction into the enclosure to cooperate with the first and second electrodes and the magnets in obtaining an ionization of the gas molecules in the enclosure by the electrical and magnetic fields in the enclosure and [to] in obtaining a movement of the ions in the enclosure to the insulating layer in the wafer at a speed to obtain a smooth and [even] uniform etching of the surface of the insulating layer at a low rate without any pits in the surface of the insulating layer.

22. (Amended): A method of etching an insulating layer in a wafer to present a clean and fresh surface on the insulation layer for a deposition on the insulating layer, including the steps of:

providing a relatively strong electrical field at first positions in an enclosure,

providing a relatively weak electrical field at second positions displaced in the enclosure from the first positions, the relatively weak electrical fields defining a capacitor with a high impedance to limit the transfer of electrical charges to the insulating layer in the wafer,

passing molecules of an inert gas through the enclosure, and

providing a magnetic field in the enclosure in a direction relative to the strong electrical field to obtain a movement of electrons in the enclosure at the positions of the relatively strong electrical field and an ionization of molecules of the inert gas by the electrons and a movement of the ions in a direction relative to the weak electrical field to obtain a movement of the ions, in accordance with the high impedance of the capacitor defined by the relatively weak electrical field, to the second electrode at a speed for etching the surface of the insulating layer on the wafer substantially uniformly without pitting the insulating layer.

23. (Amended): A method as set forth in claim 22 wherein

the relatively strong electrical field is provided in a first direction and

the relatively weak electrical field is provided in a second direction opposite to the first direction and wherein

the magnetic field is provided in a direction transverse to the first and second directions to cooperate with the relatively strong electrical field in producing a movement of the electrons in the enclosure in a helical path for facilitating the ionization of molecules of the inert gas in the enclosure.

24. (Amended): A method as set forth in claim 22 wherein

the wafer is disposed in the weak electrical field and wherein

the molecules of the inert gas are passed through the enclosure initially to positions in the relatively strong electrical field to obtain an ionization of molecules of the inert gas and subsequently through the enclosure to positions in the relatively weak electrical field to facilitate [an] a substantially uniform etching of the surface of the insulating layer on the wafer by the ions.

26. (Amended): A method as set forth in claim 2[1]2 wherein

the capacitor constitutes a first capacitor and wherein

the relatively weak electrical field is defined by the first capacitor and a second capacitor in a series circuit and wherein

the first capacitor is defined by plates constituting an electrode and the wafer and in which the plates are separated by a space in which molecules and ions of the inert gas are

disposed to define the insulator for the capacitor and to provide the first capacitor with the high impedance and wherein

a second capacitor is defined by plates constituting the wafer and the ions of the inert gas in the enclosure and wherein the plates are separated by the insulating layer in the wafer to define the insulator of the second capacitor and to provide the second capacitor with a relatively low impedance in comparison to the high impedance of the first capacitor.

28. (Amended): A method as set forth in claim 26 wherein

the wafer is disposed in the relatively weak electrical field and wherein

the molecules of the inert gas are passed through the enclosure initially through positions in the relatively strong electrical field to obtain an ionization of molecules of the inert gas and subsequently through positions in the relatively weak electrical field to facilitate [an] a substantially uniform etching of the surface of the insulating layer on the wafer by the ions and wherein

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the wafer is disposed in the relatively weak electrical field and wherein

an electrode providing the relatively weak field is spaced from, but disposed relatively close to, the wafer to cooperate with the wafer in providing a high impedance in the capacitor and a circuit including the capacitor for attracting the ions in the weak electrical field to the wafer to etch the surface of the insulating layer on the wafer without pitting the insulating layer.

29. (Amended): A method as set forth in claim 26 wherein

the capacitor constitutes a first capacitor and wherein

the first capacitor and a second capacitor are in series and wherein

the first capacitor is defined by plates constituting an electrode and the wafer and [in which] wherein the plates are separated by a space in which molecules and ions of the inert gas are disposed to define the insulator for the capacitor and to provide the high impedance and

wherein

the second capacitor is defined by plates constituting the wafer and the ions of the inert gas in the enclosure and wherein the plates are separated by the insulating layer in the wafer to define the insulator of the second capacitor[s] and to provide a relatively low impedance in comparison to the high impedance of the first capacitor and wherein

the relatively strong electrical field is provided by a first electrode and a first alternating voltage providing a relatively high negative bias on the first electrode and wherein

the relatively ~~weak electrical field is provided~~ by a second electrode and by a second alternating voltage providing a relatively low negative bias on the second electrode.

31. (Amended): A method as set forth in claim 30 wherein

the molecules of the inert gas pass through the enclosure from the strong electrical field to the weak electrical field and wherein

the magnetic field is substantially perpendicular to the strong and weak electrical fields.

36. (Amended): A method as set forth in claim 30 wherein

the second electrode and the wafer constitute plates of a first capacitor and ions and molecules of the inert gas constitute the dielectric of the first capacitor and wherein

the wafer and the ions of the inert gas constitute[s] plates of a second capacitor and wherein the insulating layer of the wafer constitutes the dielectric of the second capacitor and wherein

the first capacitor has a higher impedance than the second capacitor.

37. (Amended): A method of etching an insulating layer on a wafer having at least one socket, defined by walls in the insulating layer, to present a clean and fresh surface on the insulating layer, ~~including the walls of the socket,~~ for deposition, including the steps of:

passing molecules of an inert gas through an enclosure,

providing a strong electrical field at first positions in the enclosure to ionize molecules of the inert gas in the enclosure

providing a weak electrical field at second positions, including the positions of the wafer, in the enclosure, and

providing a magnetic field in the enclosure in a direction transverse to the directions of the first and second electrical fields in the enclosure to cooperate with the strong electrical field in producing charged particles and to cooperate with the weak electrical field in producing a transfer of the charged particles, to the surface of the insulating layer in the wafer and to the walls of the socket in the insulating layer, at a low speed to provide a weak and controlled etching of a uniform thickness from the surface of the insulating layer and the walls of the socket without pitting the surface of the insulating layer[s] or the walls of the socket.

39. (Amended): A method as set forth in claim 37, including the steps of:

disposing the wafer in the enclosure in [a] an adjacent but spaced relationship to the second electrode to provide a high impedance between the second electrode and the wafer for limiting the transfer of charged particles to the surface of the insulating layer and the walls of the socket and for providing for [an elimination] a removal of a substantially uniform thickness from the surface of the insulating layer and from the surfaces of the walls of the socket.

40. (Amended): A method as set forth in claim 37, including the steps of:

providing a first electrode to create the strong electrical field,

providing a second electrode to create the weak electrical field,

providing magnets to create the magnetic field,

the first and second electrodes and the magnets substantially defining the enclosure, and

disposing the wafer in the enclosure in a closely spaced relationship to the second electrode.

42. (Amended): A method as set forth in claim 37 including the steps of:

introducing an alternating voltage of a first particular magnitude to the first electrode to produce a strong negative DC bias on the first electrode for the creation of the strong electrical field,

introducing an alternating voltage of a second particular magnitude less than the first particular magnitude to the second electrode to produce a weak negative bias on the second electrode for the creation of the weak electrical field, and

providing a high impedance between the second electrode and the wafer and a low ~~impedance between the wafer~~ and the charged particles near the wafer to produce a transfer of charged particles with limited energy to the surface of the insulating layer and the walls of the socket in the insulating layer and to provide the weak and controlled etching of the surface of the insulating layer and the walls of the socket with a substantially uniform thickness of material from the insulating layer and the wall of the socket without pitting the surface of the insulating layer or the walls of the socket.